

WHAT IS CLAIMED IS:

1. A multiplexing and transmission  
apparatus which receives low-speed frame signals  
5 from a plurality of channels in parallel and outputs  
a high-speed serial signal, said multiplexing and  
transmission apparatus comprising:

a control pulses generating circuit which  
generates control pulses each of which corresponds  
10 to one of said channels, wherein phases of said  
control pulses are different for each channel;

channel-frame generating circuits,  
connected to said control pulses generating circuit,  
each of which receives said low-speed frame signal  
15 and outputs said low-speed frame signal in  
synchronization with said control pulse; and

a multiplexing circuit, connected to said  
channel-frame generating circuits, which multiplexes  
said low-speed frame signals into said high-speed  
20 serial signal and outputs said high-speed serial  
signal.

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2. A multiplexing and transmission  
apparatus which receives a high-speed serial signal,  
demultiplexes said high-speed serial signal into  
low-speed frame signals and outputs said low-speed  
30 frame signals to a plurality of channels in parallel,  
said multiplexing and transmission apparatus  
comprising:

a demultiplexer which demultiplexes said  
high-speed serial signal into said low-speed frame  
35 signals;

channel-frame synchronization circuits,  
connected to said demultiplexer, each of which

receives said low-speed frame signal, generates a frame pulse corresponding to said low-speed frame signal, and outputs said low-speed frame signal;

5 a switching circuit, connected to said channel-frame synchronization circuits, which receives said low-speed frame signals and sends each of said low-speed frame signals to an appropriate port of said channel; and

10 a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits.

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3. A multiplexing and transmission apparatus which receives send low-speed frame signals from a plurality of send channels in parallel, outputs a send high-speed serial signal, receives a receive high-speed serial signal, demultiplexes said receive high-speed serial signal into receive low-speed frame signals and outputs said receive low-speed frame signals to a plurality of receive channels in parallel, said multiplexing and transmission apparatus comprising:

20 a control pulses generating circuit which generates control pulses each of which corresponds to one of said send channels, wherein phases of said control pulses are different for each send channel;

30 channel-frame generating circuits, connected to said control pulses generating circuit, each of which receives said send low-speed frame signal, and outputs said send low-speed frame signal in synchronization with said control pulse;

35 a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes

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said send low-speed frame signals into said send high-speed serial signal and outputs said send high-speed serial signal;

5 a demultiplexer which demultiplexes said receive high-speed serial signal into said receive low-speed frame signals;

channel-frame synchronization circuits, connected to said demultiplexer, each of which receives said receive low-speed frame signal,  
10 generates a frame pulse corresponding to said receive low-speed frame signal, and outputs said receive low-speed frame signal;

a switching circuit, connected to said channel-frame synchronization circuits, which  
15 receives said receive low-speed frame signals and sends each of said receive low-speed frame signals to an appropriate port of said receive channel; and

a switch controller circuit which controls said switching circuit according to said frame  
20 pulses output from said channel-frame synchronization circuits.

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4. The multiplexing and transmission apparatus as claimed in claim 1, said multiplexing and transmission apparatus further comprising:

synchronization pattern inserting circuits  
30 each of which inserts a frame synchronization pattern into said low-speed frame signal.

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5. The multiplexing and transmission apparatus as claimed in claim 1, wherein time

duration on which said control pulses are generated for every channel is smaller than time duration of channel-frame format.

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6. The multiplexing and transmission apparatus as claimed in claim 5, said control pulses  
10 generating circuit comprising:  
a control clock generator;  
a DC voltage generator;  
a selector which outputs said control  
pulses sequentially for each channel according to  
15 control clock supplied from said control clock generator, said control pulses generated according to signals supplied from said DC voltage generator.

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7. The multiplexing and transmission apparatus as claimed in claim 2, wherein each of said channel-frame synchronization circuits  
25 establishes frame synchronization on a channel-by-channel basis and outputs said frame pulse which indicates head position of said low-speed frame signal; and  
said switch controller circuit identifies  
30 channel numbers of said low-speed frame signals according to time difference for receiving said frame pulses, and controls said switching circuit.

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8. The multiplexing and transmission

apparatus as claimed in claim 7, said switch  
controller circuit comprising:

5 a shift register which receives said frame  
pulses in parallel and shifts each of said frame  
pulses;

exclusive-OR circuits each of which is  
connected to said shift register and provided for  
each frame pulse;

10 demultiplexers each of which is connected  
to said exclusive-OR circuit and outputs a pattern  
indicating time position of said frame pulse;

a reset pulse generating circuit which  
initializes said demultiplexers according to  
receiving state of said frame pulse.

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9. A computer readable medium storing  
20 program code for causing a computer to control a  
switching circuit in an multiplexing and  
transmission apparatus which receives a high-speed  
serial signal and demultiplexes said high-speed  
serial signal into low-speed frame signals, wherein  
25 said switching circuit assigns each of said low-  
speed frame signals to an appropriate port of a  
channel, said computer readable medium comprising:

30 program code means for receiving and  
storing frame pulses indicating head positions of  
said low-speed frame signals;

program code means for checking whether  
said frame pulses for every channel are stored;

35 program code means for reading said frame  
pulses and identifying receiving order of said low-  
speed frame signals; and

program code means for controlling said  
switching circuit on the basis of said receiving

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order so that said switching circuit assigns each of said low-speed frame signals to an appropriate port of a channel.

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10. A multiplexing and transmission method used in an apparatus which receives low-speed frame signals from a plurality of channels in parallel and outputs a high-speed serial signal, said multiplexing and transmission method comprising the steps of:

generating control pulses each of which corresponds to one of said channels, wherein phases of said control pulses are different for each channel;

receiving said low-speed frame signal and outputting said low-speed frame signal in synchronization with said control pulse for each of said low-speed frame signals; and

multiplexing said low-speed frame signals into said high-speed serial signal and outputting said high-speed serial signal.

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11. A multiplexing and transmission method used in an apparatus which receives a high-speed serial signal, demultiplexes said high-speed serial signal into low-speed frame signals and outputs said low-speed frame signals to a plurality of channels in parallel, said multiplexing and transmission method comprising the steps of:

demultiplexing said high-speed serial signal into said low-speed frame signals;

generating, for each of said low-speed frame signals, a frame pulse corresponding to said low-speed frame signal;

switching each of said low-speed frame signals to an appropriate port of said channel according to signals generated from said frame pulses.

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12. A multiplexing and transmission method used in an apparatus which receives send low-speed frame signals from a plurality of send channels in parallel, outputs a send high-speed serial signal, receives a receive high-speed serial signal, demultiplexes said receive high-speed serial signal into receive low-speed frame signals and outputs said receive low-speed frame signals to a plurality of receive channels in parallel, said multiplexing and transmission method comprising the steps of:

generating control pulses each of which corresponds to one of said send channels, wherein phases of said control pulses are different for each send channel;

receiving said send low-speed frame signal and outputting said send low-speed frame signal in synchronization with said control pulse for each of said send low-speed frame signals; and

multiplexing said send low-speed frame signals into said send high-speed serial signal and outputting said send high-speed serial signal;

demultiplexing said receive high-speed serial signal into said receive low-speed frame signals;

generating, for each of said receive low-

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generator.

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16. The multiplexing and transmission method as claimed in claim 11, said multiplexing and transmission method further comprising the step of:

10 establishing frame synchronization on a channel-by-channel basis and outputting said frame pulse which indicates head position of said low-speed frame signal for each of said low-speed frame signals; and

15 identifying channel numbers of said low-speed frame signals according to time difference of said frame pulses, and performing said step of switching according to said time difference.

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17. The multiplexing and transmission method as claimed in claim 16, said multiplexing and transmission method further comprising the steps of:

25 shifting each of said frame pulses; performing an exclusive-OR operation on said frame pulses;

30 generating a pattern indicating time position of said frame pulse for each of said frame pulses.

18. A method used in a computer to control  
35 a switching circuit in an multiplexing and transmission apparatus which receives a high-speed serial signal and demultiplexes said high-speed

5                   receiving and storing frame pulses  
indicating head positions of said low-speed frame  
signals;

10           reading said frame pulses and identifying  
receiving order of said low-speed frame signals; and

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